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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,506	04/12/2004	John V. Sell	5500-98000	3040

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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,506	SELL, JOHN V.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-12-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-9, 11-17 & 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,801,208 B2 to Keshava et al. in view of U.S. Patent No. 6,819,321 B1 to Hsieh et al. and further in view of U.S. Patent No. 6,825,848 B1 to Fu et al.

a. Regarding claim 1, Keshava et al. **discloses** processor (processor core 10, Fig. 1); a graphics unit (graphics engine 12, Fig. 1); a memory (main memory 16) coupled to the processor (processor core 10, Fig. 1) and the graphics unit (graphics engine 12, Fig. 1); and a shared cache (L2 cache memory 24) (...a cache memory may be shared between a processor core and a graphics engine...col. 1, lines 64-67; col. 2, lines 1-37...processor core 10 and graphics engine 12...coupled to L2 cache memory 24...). However, Keshava et al. **does not disclose** partitioning of images into a plurality of subset areas; tracking the number of times data is considered from the subset areas or the determination of cacheable data from the subset area. Hsieh et al. **discloses** a method and apparatus for graphics data in a tiled graphics architecture thus partitioning graphics data to be rendered (...in order to

make...efficient use of the graphics cache memory, 3D primitives are sorted into bits...technique is...tiling...col. 1, lines 30-35;...the graphics controller...reads the...data out of the bin storage...primitive...is divided to create...in bins...the bin can be rendered...col. 1, lines 55-67; col. 2, lines 1-15; col. 3, lines 1-67; col. 4, lines 1-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Keshava et al. graphics controller with the "tiling technique for partitioning of image data" as taught by Hsieh et al. **because** it reduces cache misses and improves graphics memory bandwidth utilization, thereby improving overall computer system performance (col. 3, lines 14-18). However, Keshava-Hsieh combination **fails to disclose** tracking the number of times subset areas is considered during rendering of a first image; and determining whether the subset area is cacheable. Fu et al. **discloses** multilevel graphics processing cache wherein reference counters and age status stacks are utilized which keep track of cache hits and make decisions for keeping a cache line in terms of least recently used cache lines (col. 2, lines 30-67; col. 3, lines 1-19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Keshava-Hsieh combination with the features "reference counters and age status stacks" as taught by Fu et al. **because** it provides for coherent graphics cache resulting in reduced memory access time.

b. Regarding claims 2-4, Fu et al. **discloses** use of reference counters and age status stack for keeping cache entries tuned for least recently used cache lines and

availability of the graphics data in the first and second caches. Fu et al. thus tracks how often a cache line is used (via reference counters) and manages least recently used cache line (via age status stacks), and keeps/discards cache lines accordingly (col. 2, lines 15-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Keshava-Hsieh combination with the features "reference counters and age status stacks for cache lines in determining which cache lines to keep/discard" as taught by Fu et al. **because** it results in coherent graphics cache resulting in reduced memory access time.

c. Regarding claim 5, Fu et al. **discloses** resetting the count values and incrementing an entry count (...the first and second reference counters are reset or incremented based on...graphics data in the...caches...col. 2, lines 53-63).

d. Regarding claim 6, Keshava et al. is dynamically allocating L2 cache between graphics engine and re-allocating it the processor core during graphics processing. Keshava et al. thus is monitoring L2 cache sharing between graphics engine and the processor core. Keshava et al. further **discloses** evicted data from L2 cache being used by the graphics are not lost and are stored to either the cache memory, the main memory, and/or disk. Although, Keshava is not explicitly disclosing cache entries evicted from the graphical cache to the shared cache , L2 cache, but it does indicate evicted entries if they are determined to be cacheable to be stored in a cache memory. Therefore, it would have been obvious to a person of

ordinary skill in the art at the time invention was made to keep evicted entries from the graphical cache 18 in the shared cache L2 **because** it will result in shorter memory access time making processing time faster.

e. Regarding claim 7, Keshava-Hsieh **does not disclose** explicit cacheable data determination. Fu et al. uses reference counters and age status stacks for making cacheable data determination (col. 2, lines 15-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Keshava-Hsieh combination with the feature "reference counters and age status stacks for cache lines in determining which cache lines to keep/discard" as taught by Fu et al. **because** it results in coherent graphics cache resulting in reduced memory access time.

f. Regarding claim 8, Fu et al. **discloses** use of cache flags (col. 2, lines 15-65).

g. Regarding claim 9, Keshava-Hsieh combination **is silent about** threshold being programmable. Fu et al. uses reference counters and age status stacks for making cacheable data determination (col. 2, lines 15-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Keshava-Hsieh combination with the feature "reference counters and age status stacks for cache lines in determining which cache lines to keep/discard and using the values of counters/age status stacks for establishing a threshold" as taught by Fu et al. **because** it results in coherent graphics cache resulting in reduced memory access time.

h. Regarding claim 11, it is similar in scope to claim 1 above and is rejected under the same rationale.

i. Regarding claim 12, it is similar in scope to claim 2 above and is rejected under the same rationale.

j. Regarding claim 13, it is similar in scope to claim 3 above and is rejected under the same rationale.

k. Regarding claim 14, it is similar in scope to claim 6 above and is rejected under the same rationale.

l. Regarding claim 15, it is similar in scope to claim 5 above and is rejected under the same rationale.

m. Regarding claim 16, it is similar in scope to claim 7 above and is rejected under the same rationale.

n. Regarding claim 17, it is similar in scope to claim 9 above and is rejected under the same rationale.

o. Regarding claim 19, it is similar in scope to claim 1 above and is rejected under the same rationale.

p. Regarding claim 20, it is similar in scope to claim 2 above and is rejected under the same rationale.

q. Regarding claim 21, it is similar in scope to claim 3 above and is rejected under the same rationale.

r. Regarding claim 22, it is similar in scope to claim 4 above and is rejected under the same rationale.

s. Regarding claim 23, it is similar in scope to claim 5 above and is rejected under the same rationale.

t. Regarding claim 24, it is similar in scope to claim 6 above and is rejected under the same rationale.

u. Regarding claim 25, it is similar in scope to claim 9 above and is rejected under the same rationale.

3. Claim 10, 18 & 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,801,208 B2 to Keshava et al. in view of U.S. Patent No. 6,819,321 B1 to Hsieh et al. and further in view of U.S. Patent No. 6,825,848 B1 to Fu et al., and further in view of U.S. Patent No. 6,681,297 B2 to Chauvel et al.

a. Regarding claim 10, Keshava-Hsieh-Fu combination **is silent about** value of the threshold being responsive in part to the processor data miss rate in the shared cache. Chauvel et al. **discloses** a cache configuration based on average miss rate to reduce the miss rate from a cache (col. 2, lines 1-35; col. 17, lines 5-36; Fig. 9). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Keshava-Hsieh-Fu combination with the feature "miss rate monitoring and reconfiguring the system if the miss rate exceeds a threshold" as taught by Chauvel et al. **because** it results in a efficient cache design for the system resulting in reduced memory access times.

b. Regarding claim 18, it is similar in scope to claim 10 above and is rejected under the same rationale.

c. Regarding claim 26, it is similar in scope to claim 10 above and is rejected under the same rationale.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(571) 272-7778**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

dks

March 18, 2005

Kee M. Tung
Primary Examiner